ABSTRACT

An apparatus and method for reducing the power consumption of a memory integrated circuit during a period of power down mode operation by interrupting the clocking transitions of a delay line. A memory integrated circuit may include a delay lock loop including a plurality of delay elements connected to one another in series and adapted to delay propagation of the signal of a free running clock. When the delayed signal is not required, as during a period of power down mode operation, the free running clock signal is prevented from reaching the delay lock loop. Consequently the delay elements do not toggle, and power associated with delay element toggling is saved.